LISTING OF CLAIMS

Claim 1 (Cancelled)

Claim 2 (Original): A method for compensating for bitline leakage in a memory system, the method comprising:

detecting a first voltage on a bitline in a first memory array;

applying a second voltage to a bitline in a second memory array, the second voltage having substantially the same amplitude as the first voltage;

detecting a leakage current on the bitline of the second memory array;

applying an incremental current to the bitlines of the first memory array substantially equal to the detected current during programming of the first memory array.

Claim 3 (Original): A memory comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells and including a plurality of bitlines, each of said plurality of bitlines being coupled to a corresponding group of said plurality of memory cells;

a first circuit having an input coupled to a bitline of a first one of the memory arrays and having an output coupled to a bitline of a second one of the memory arrays to apply a voltage on said bitline of said second memory array equal to a voltage on said bitline of the first memory array during programming of said first memory array;

a second circuit coupled to the bitline of the second memory array to measure current on said bitline; and

a current source coupled to the bitline of the first memory array to provide a current thereto in response to the detected current on the bitline of the second memory array.

Claim 4 (Original): The memory of claim 3,

wherein the first memory array is an operational memory array and said second memory array is a non-operational memory array.

Claim 5 (Original): The memory of claim 3,

wherein the first memory array is an operational memory array and the second memory array is a dummy memory array.

Claim 6 (Original): The memory of claim 3,

wherein the first circuit comprises an operational amplifier including a first input coupled to the bitline of the first memory array, including a second input coupled to the bitline of the second memory array, and including an output,

wherein the second circuit comprises a first transistor including first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said first terminal being coupled to the output of said operational amplifier, said second terminal being coupled to the bitline of the second memory array, said gate being coupled to said second terminal,

wherein the current source comprises a second transistor including first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said first terminal being coupled to the first terminal of the first transistor, said second terminal being coupled to the bitline of the first memory array, said gate being coupled to the second terminal of the first transistor.

Claim 7 (Original): The memory of claim 3,

wherein the first circuit comprises an operational amplifier including a first input coupled to the bitline of the first memory array, including a second input coupled to the bitline of the second memory array, and including an output, and further comprises an NMOS transistor including first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said second terminal being coupled to the bitline of the second memory array, said gate being coupled to the output of the operational amplifier,

wherein the second circuit comprises a first PMOS transistor including first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said first terminal being coupled to a supply voltage node, said second terminal being coupled to the first terminal of the NMOS transistor, said gate being coupled to said second terminal,

wherein the current source comprises a second PMOS transistor including first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said first terminal being coupled to the supply voltage node, said second terminal being coupled to the bitline of the first memory array, said gate being coupled to the second terminal of the first PMOS transistor.

Claim 8 (Original): The memory of claim 3,

wherein said first circuit has a plurality of second outputs coupled to a corresponding bitline of said second memory array to apply a voltage on said corresponding bitline of said second memory array equal to said voltage on said bitline of the first memory array,

wherein said second circuit is coupled to said corresponding bitlines of the second memory array to measure current on said corresponding bitlines, and

wherein said current source provides said current to the bitline of the first memory array in response to the detected currents on the bitlines of the second memory array.

Claim 9 (Original): The memory of claim 8,

wherein said first circuit comprises a plurality of operational amplifiers and a plurality of first NMOS transistors, each operational amplifier includes a first input coupled to a corresponding bitline of the first memory array, including a second input coupled to a corresponding bitline of the second memory array, and including an output, each NMOS transistor includes first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said second terminal being coupled to a corresponding bitline of the second memory array, said gate being coupled to the output of a corresponding operational amplifier,

wherein the second circuit comprises a plurality of first PMOS transistors, a plurality of second PMOS transistors, a third PMOS transistor, a second NMOS transistor, and a third NMOS transistor, each of the first, second and third PMOS transistors and of the second and third NMOS transistors include first and second terminals with a channel therebetween and including a gate for controlling current in said channel, said first terminal of the first PMOS transistor being coupled to an output of a corresponding operational amplifier of the first circuit, said second terminal of the first PMOS transistor being coupled to a corresponding bitline of the

second memory array, said gate of the first PMOS transistor being coupled to said second terminal, said first terminal of the second PMOS being coupled to the first terminal of the corresponding first PMOS transistor, said second terminal of the second PMOS being coupled to a summation node, said gate of the second PMOS being coupled to a second terminal of said corresponding first PMOS transistor, said first terminal of the third PMOS transistor being coupled to a supply voltage node, said second terminal of the third PMOS transistor being coupled to said gate of the third PMOS transistor, said first terminal of the second NMOS transistor being coupled to the summation node, said second terminal of the second NMOS transistor being coupled to a ground node, said gate of the second NMOS transistor being coupled to said first terminal of the second NMOS transistor, said first terminal of the third NMOS transistor being coupled to the second terminal of the third PMOS transistor, said second terminal of the third NMOS transistor being coupled to the ground node, said gate of the third NMOS transistor being coupled to the first terminal of the second NMOS transistor, said second NMOS transistor having a multiplier relative to the third NMOS transistor substantially equal to the number of second PMOS transistors in said second circuit,

wherein the current source comprises a plurality of fourth PMOS transistors.

Claim 10 (Original): A memory comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells and including a plurality of bitlines, each of said plurality of bitlines being coupled to a corresponding group of said plurality of memory cells;

a current source having an output for providing a first current in a first mode and having a second output to provide a second current to a bitline of the first memory array in a second mode; and

the detector having a first input coupled to a bitline of a second memory array, having a second input coupled to the first output of the current source to receive said first current and having an output coupled to said bitline of the first memory array to apply a voltage on the bitline of the first memory array substantially equal to the voltage on the bitline of the second memory array in the first mode, the first and second currents being substantially equal and the first and second modes, respectively.